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Application / Conf. No.	09/649,437 / 6896					
Filing Date	August 23, 2000					
First Named Inventor	Bart Reynolds					
Art Unit	2123					
Examiner Name	Eduardo Garcia Otero					
Attorney Docket Number	X-1770 US					

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X Ass	ignee of record of tement under 37 C	the entire int FR 3.73(b) is	erest. <i>enclo</i>	See CFR 3. sed. (Form I	.71 PTO/S	SB/96).
	SIGNATURE of A	pplicant or As	signe	of Record	_	_
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Signature	Humunk	teenle	7			
Date	June 22, 2004		(_
NOTE: Signatures o are required. Submit	f all the inventors or as multiple forms if more	ssignees of reco than one signatu	rd of th re is re	e entire interes quired, see belo	t or the	eir representative(s)
Total of	forms are	submitted.				

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		<u>STATEMENT</u>	UNDER 37 CFR	3.73(b)
Applicant/l	Patent Owner:	Xilinx, Inc.		
Application	n No./Patent No.:	09/649,437	Filed/Issue Dat	e:
Entitled: _	Method and Ap Logic Design	paratus for Specify	ving Addressability	y and Bus Connections in a
	Xilinx, Inc.	<u>,</u> a	Corporation	· ,
	(Name of Assignee)	(Type of A	ssignee, e.g., corporation, pa	rtnership, university, government agency, etc.)
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	-	entified above by virtue of	either:	Technology Center 210
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The under	signed (whose title is s	upplied below) is empowe	ered to sign this statement	on behalf of the assignee.
	June 22, 2004		Him	ef la
	Date 22, 2004			Signature
				nas R. Lavelle
		(XXI)	r v	or printed name
		1 (0 • 0	Vice Pre	esident, Secretary
Y-1770 IIS				Title